WHAT IS CLAIMED IS:

1. An electrically erasable and programmable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

spaced-apart first and second regions formed in the substrate and having a second conductivity type different from the first conductivity type, with a channel region therebetween;

a conductive select gate formed over and insulated from the substrate, the select gate extending over a first portion of the channel;

a conductive floating gate formed as a spacer over and insulated from the substrate, the floating gate including:

a bottom surface extending over a second portion of the channel region, and

first and second side surfaces extending from the bottom surface; and

a conductive control gate formed over and insulated from the floating gate, the control gate includes:

a first portion disposed adjacent to the first floating gate side surface, and

a second portion disposed adjacent to the second floating gate side surface.

2. The device of claim 1, wherein the floating gate second side surface has a first portion disposed adjacent to and is insulated from a side surface of the select gate, and a second portion disposed adjacent to and insulated from the control gate second portion.

3. The device of claim 2, wherein the second portion of the floating gate second side surface is disposed over and is insulated from the select gate.

4. The device of claim 2, further comprising:

a first spacer of insulation material formed between the select gate side surface and the first portion of the floating gate second side surface.

5. The device of claim 4, wherein the first spacer is further formed between the control gate second portion and the second portion of the floating gate second side surface.

6. The device of claim 4, further comprising:

a second spacer of insulation material formed between the control gate second portion and the second portion of the floating gate second side surface.

7. The device of claim 1, wherein at least a portion of the floating gate bottom surface is disposed over and insulated from at least a portion of the first region.

8. The device of claim 1, wherein the control gate first portion is disposed over and insulated from the first region.

9. The device of claim 8, wherein the control gate second portion is disposed over and insulated from the select gate.

10. The device of claim 1, wherein the control gate has a side surface aligned with a second side surface of the select gate.

11. A method of making a memory device on a semiconductor substrate of a first conductivity type, comprising the steps of:

forming spaced-apart first and second regions in the substrate that have a second conductivity type different from the first conductivity type, wherein a channel region is defined in the substrate between the first and second regions;

forming a conductive select gate over and insulated from the substrate, wherein the select gate extends over a first portion of the channel and has a first height;

forming a conductive floating gate spacer over and insulated from the substrate, wherein the floating gate includes:

a bottom surface extending over a second portion of the channel region, and

first and second side surfaces extending from the bottom surface to a height greater than the first height; and

forming a conductive control gate over and insulated from the floating gate, wherein the control gate includes a first portion disposed adjacent to the first floating gate side surface and a second portion disposed adjacent to the second floating gate side surface.

12. The method of claim 11, wherein the floating gate second side surface includes:

a first portion disposed adjacent to and insulated from a side surface of the select gate; and

a second portion disposed adjacent to and insulated from the control gate second portion.

13. The method of claim 12, wherein the second portion of the floating gate second side surface is disposed over and is insulated from the select gate.

14. The method of claim 12, further comprising the step of:

forming a first spacer of insulation material between the select gate side surface and the first portion of the floating gate second side surface.

15. The method of claim 14, wherein the first spacer is further formed between the control gate second portion and the second portion of the floating gate second side surface.

16. The method of claim 14, further comprising the step of:

forming a second spacer of insulation material between the control gate second portion and the second portion of the floating gate second side surface.

17. The method of claim 11, wherein at least a portion of the floating gate bottom surface is disposed over and insulated from at least a portion of the first region.

18. The method of claim 11, wherein the control gate first portion is disposed over and insulated from the first region.

19. The method of claim 18, wherein the control gate second portion is disposed over and insulated from the select gate.

20. The method of claim 11, wherein the control gate has a side surface aligned with a second side surface of the select gate.

21. The method of claim 11, wherein the formation of the control gate further includes the steps of:

selecting a desired capacitive coupling ratio between the floating gate and the control gate; and

forming the control gate second portion with a predetermined height for achieving the desired capacitive coupling ratio.

22. The method of claim 11, wherein the formation of the spaced apart first and second regions is performed simultaneously by the same ion implantation process.

23. A method of making a memory device on a semiconductor substrate of a first conductivity type, comprising the steps of:

forming spaced-apart first and second regions in the substrate that have a second conductivity type different from the first conductivity type, wherein a channel region is defined in the substrate between the first and second regions;

forming a first layer of insulating material on substrate;

forming a select gate on the first insulating layer, wherein the select gate is positioned over a first portion of said channel;

forming a second layer of insulating material on the select gate;

forming a layer of material on the second layer of insulating material;

forming a floating gate spacer of conductive material adjacent to and insulated from the select gate and adjacent to the layer of material, wherein the floating gate includes:

a bottom surface extending over a second portion of the channel region, and

first and second side surfaces extending from the bottom surface;

removing the layer of material; and

forming a conductive control gate over and insulated from the floating gate and over the second insulating layer, wherein the control gate includes a first portion disposed adjacent to and insulated from the first floating gate side surface and a second portion disposed adjacent to and insulated from the second floating gate side surface.

24. The method of claim 23, wherein the floating gate second side surface includes:

a first portion disposed adjacent to and insulated from a side surface of the select gate; and

a second portion disposed adjacent to and insulated from the control gate second portion.

25. The method of claim 24, further comprising the step of:

removing a side portion of the layer of material before the formation of the floating gate spacer, so that the second portion of the floating gate second side surface extends over the select gate.

26. The method of claim 24, wherein:

the removal of the layer of material forms a recess over the second layer of insulating material and adjacent to the second portion of the floating gate second side surface; and

the formation of the control gate includes filling at least a portion of the recess with conductive material to form the second portion of the control gate.

27. The method of claim 26, further comprising the step of:

selecting a size of the control gate second portion by selecting a thickness of the layer of material for dictating the size of the recess filled by the control gate second portion.

28. The method of claim 24, wherein the second portion of the floating gate second side surface is disposed over and is insulated from the select gate.

29. The method of claim 24, further comprising the step of:

forming a first spacer of insulation material between the select gate side surface and the first portion of the floating gate second side surface.

30. The method of claim 29, wherein the first spacer is further formed between the control gate second portion and the second portion of the floating gate second side surface.

31. The method of claim 29, further comprising the step of:

forming a second spacer of insulation material between the control gate second portion and the second portion of the floating gate second side surface.

32. The method of claim 23, wherein at least a portion of the floating gate bottom surface is disposed over and insulated from at least a portion of the first region.

33. The method of claim 32, wherein the control gate first portion is disposed over and insulated from the first region.

34. The method of claim 33, wherein the control gate second portion is disposed over and insulated from the select gate.

35. The method of claim 23, wherein the control gate has a side surface aligned with a second side surface of the select gate.

36. The method of claim 23, wherein the formation of the control gate further includes the steps of:

selecting a desired capacitive coupling ratio between the floating gate and the control gate; and

forming the control gate second portion with a predetermined height for achieving the desired capacitive coupling ratio.

37. The method of claim 23, wherein the formation of the spaced apart first and second regions is performed simultaneously by the same ion implantation process.

38. A method of designing an electrically erasable and programmable memory device formed on a substrate of semiconductor material of a first conductivity type, the device including spaced-apart first and second regions formed in the substrate with a second conductivity type different from the first conductivity type and with a channel region therebetween, a conductive select gate formed over and insulated from the substrate and extending over a first portion of the channel, a conductive floating gate formed as a spacer over and insulated from the substrate and having a bottom surface extending over a second portion of the channel region and first and second side surfaces extending from the bottom surface, and a conductive control gate formed over and insulated from the floating gate with a first portion disposed adjacent to the first floating gate side surface and a second portion disposed adjacent to the second floating gate side surface, wherein the improvement comprises the steps of:

selecting a desired capacitive coupling ratio between the floating gate and the control gate; and

adjusting a height of the control gate second portion to achieve the desired capacitive coupling ratio.

39. An electrically erasable and programmable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

spaced-apart first and second regions formed in the substrate and having a second conductivity type different from the first conductivity type, with a channel region therebetween;

a conductive select gate formed over and insulated from the substrate, the select gate extending over a first portion of the channel;

a conductive floating gate formed as a spacer over and insulated from the substrate, the floating gate including:

a bottom surface extending over a second portion of the channel region, and

first and second side surfaces extending from the bottom surface; and

a conductive control gate formed over and insulated from the floating gate, the control gate includes:

a first portion disposed adjacent to the first floating gate side surface, and

a second portion disposed adjacent to the second floating gate side surface;

wherein the control gate is formed by the process of:

selecting a desired capacitive coupling ratio between the floating gate and the control gate; and

forming the control gate second portion with a predetermined height for achieving the desired capacitive coupling ratio.

40. The device of claim 39, wherein the floating gate second side surface has a first portion disposed adjacent to and is insulated from a side surface of the select gate, and a second portion disposed adjacent to and insulated from the control gate second portion.

41. The device of claim 40, wherein the second portion of the floating gate second side surface is disposed over and is insulated from the select gate.

42. The device of claim 40, wherein the control gate first portion is disposed over and insulated from the first region.

43. The device of claim 42, wherein the control gate second portion is disposed over and insulated from the select gate.

44. The device of claim 40, wherein the control gate has a side surface aligned with a second side surface of the select gate.